Extremely-Low-Power Electron Devices: TFETs and NEM Devices

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Outline

Introduction (1)

❖ Education

- BS: EE, Seoul National Univ. (1996 - 2000)
- MS: EE, Seoul National Univ. (2000 - 2002)
- PhD: EE, Seoul National Univ. (2002 - 2006)

❖ Work Experience

- Post-Doctor/Visiting Scholar: EECS, UC Berkeley (2006-2006) (2014 - 2015)
- Professor: EE, Sogang Univ. (2008 – 2022)
- Associate Professor: ECE, Seoul National Univ. (2022 – present)
- Chair: IEEE EDS Seoul Section Chapter
- Chair: Research Council of Semiconductor Devices & Materials, IEIE

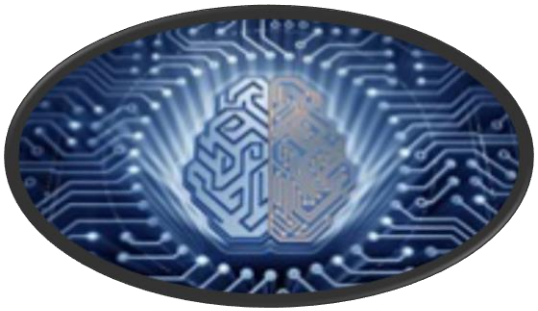
Introduction (2)

Extremely-Low-Power & High-Density

Nano-CMOS devices
Emerging electron devices
Next-generation memory devices
Brain-inspired computing devices

More Functionality & Monolithic 3D (M3D) Integration

M3D CMOS-TFET-NEM reconfigurable logic systems
Process-in-memory (PIM)
Content addressable memory



- Multi-gate MOSFET
- Nanowire MOSFET
- Nanosheet MOSFET
- Tunnel FET
- NCFET
- NEM relay

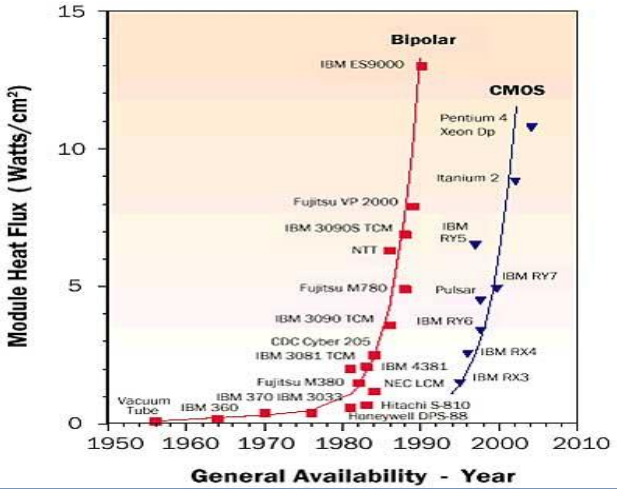
Hyper-intelligent semiconductor devices in terms of density, power and functionality

- VNAND flash
- DRAM
- M3D CMOS-TFET-NEM RL circuits
- PIM devices
- Nano-CAM

Extremely-Low-Power Devices

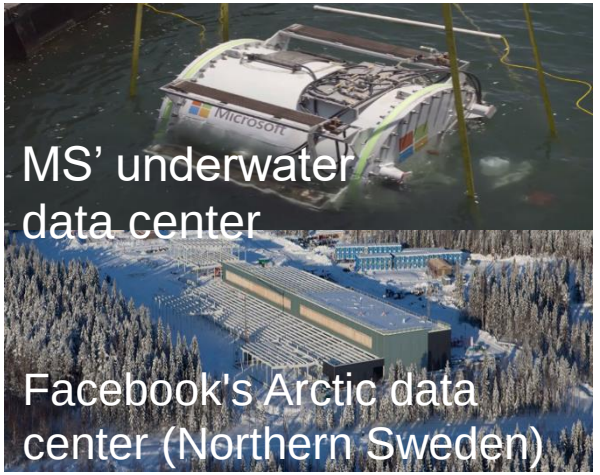
Power Rules!: Power Consumption Limits Performance & Functionality

Lower perf./reliability due to heat generation

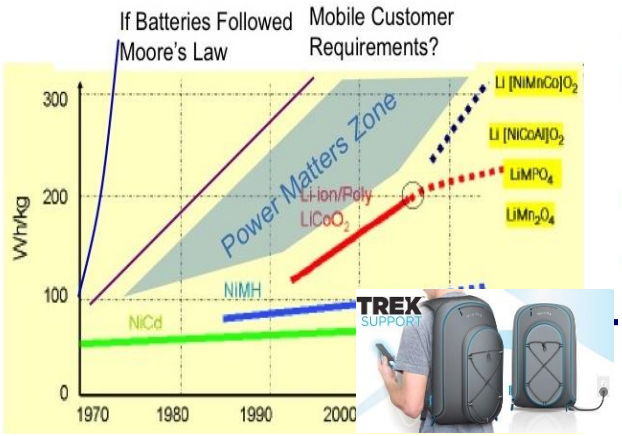


Limited power supply

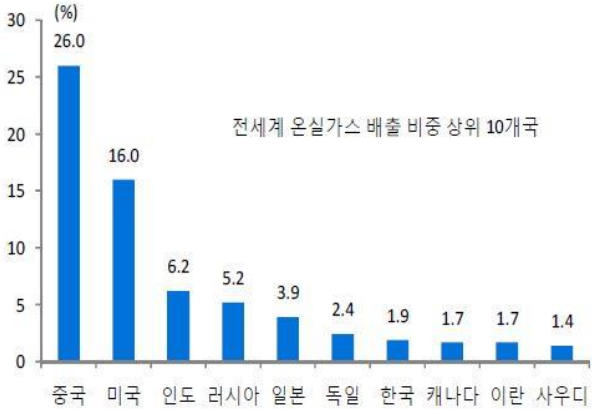
Data center power consumption



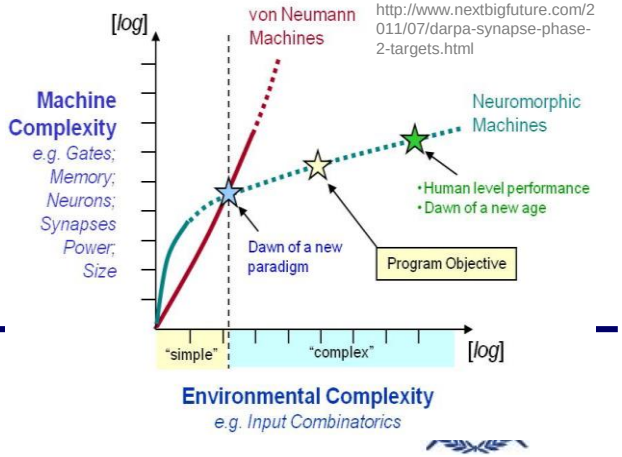
Limited battery time



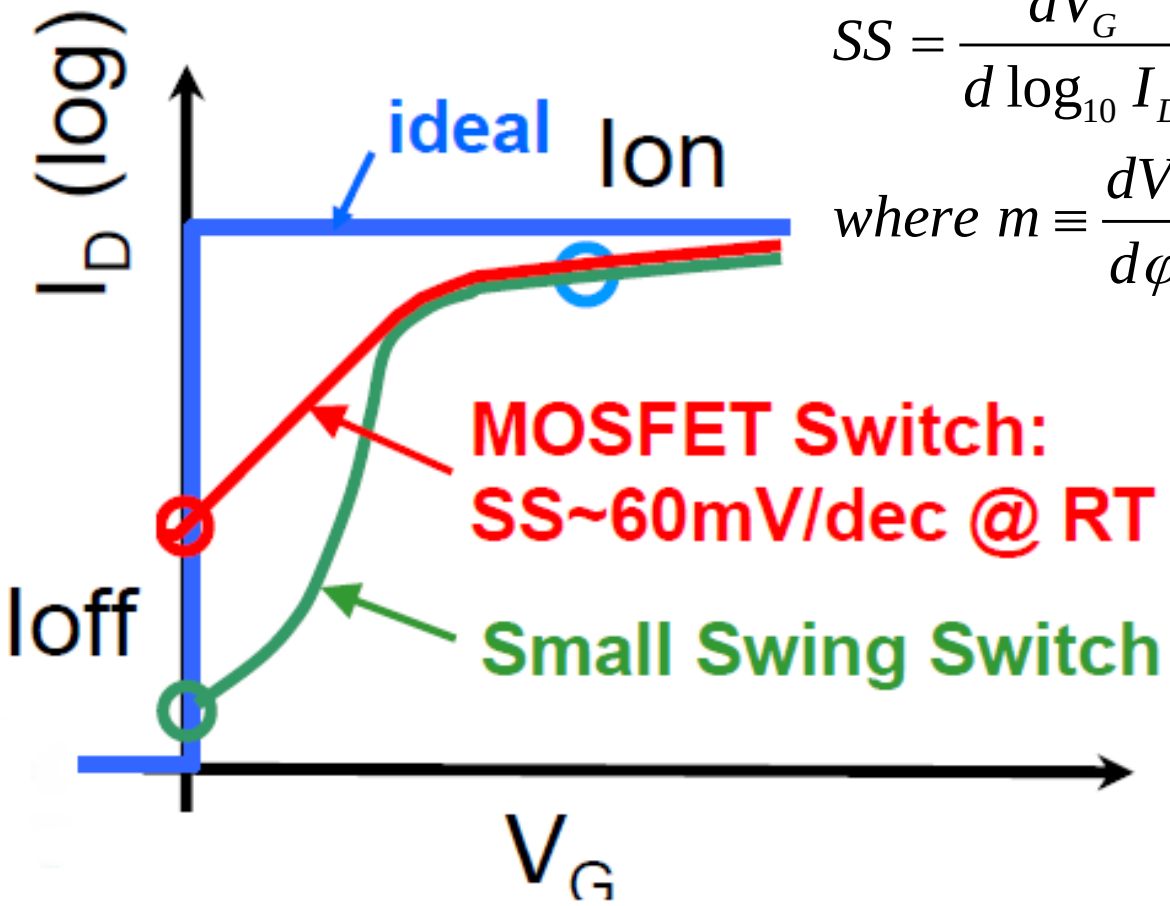
Global warming



von Neumann limit

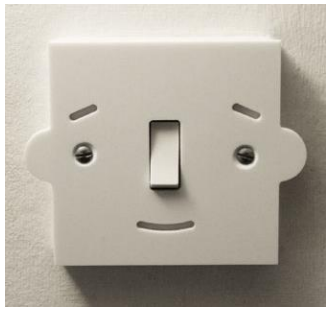


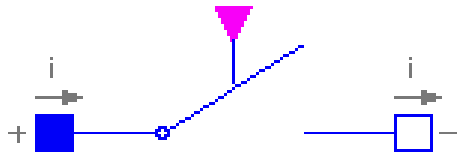
Ideal Switches



$$SS = \frac{dV_G}{d\log_{10} I_D} = \frac{dV_G}{d\varphi_s} \cdot \frac{d\varphi_s}{d\log_{10} I_D} = m \cdot n$$

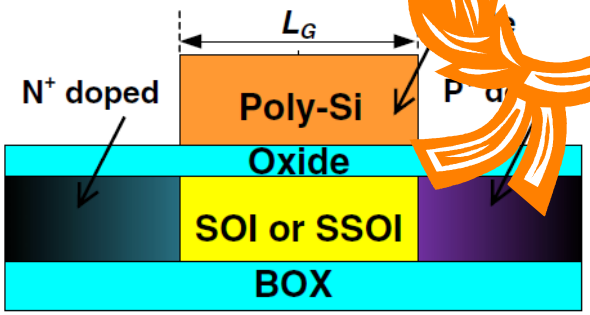
$$where\ m \equiv \frac{dV_G}{d\varphi_s}\ \&\ n \equiv \frac{d\varphi_s}{d\log_{10} I_D}$$





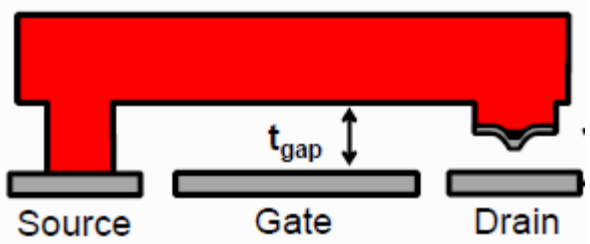
Abrupt Switching Devices

Tunnel FET



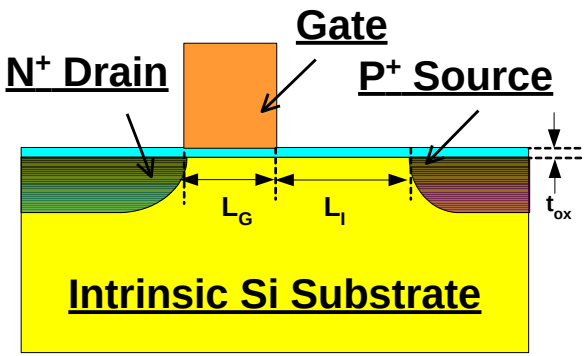
<IEDM, IEEE EDL ...>

NEM device



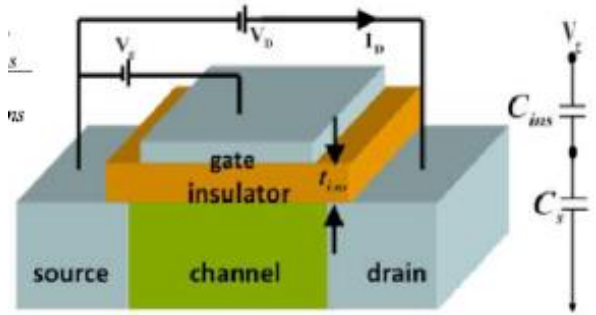
<IEDM, IEEE EDL ...>

<IEDM, IEEE EDL ...>



I-MOS

<Nano Letters ...>

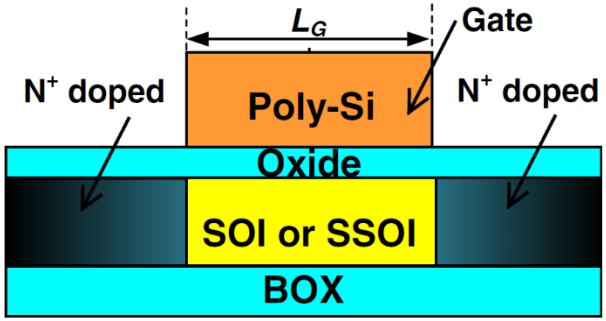


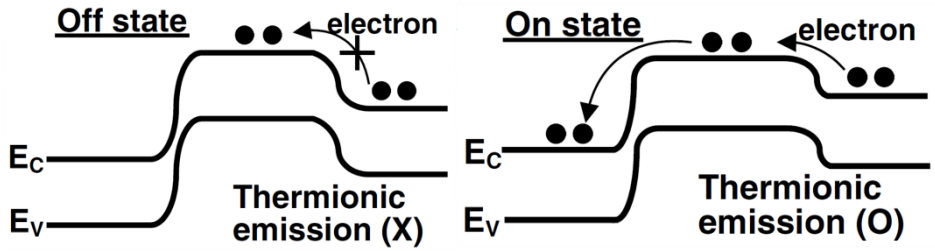
Negative cap. FET

Tunnel FETs (TFETs) (1)

MOSFET

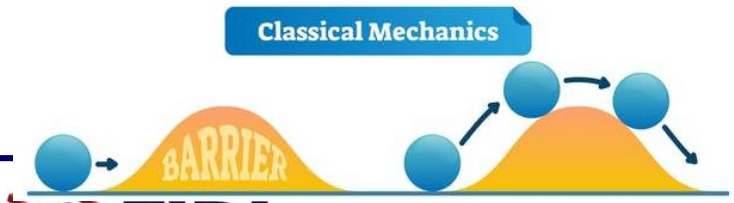
$$SS = 2.3\frac{kT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right)$$





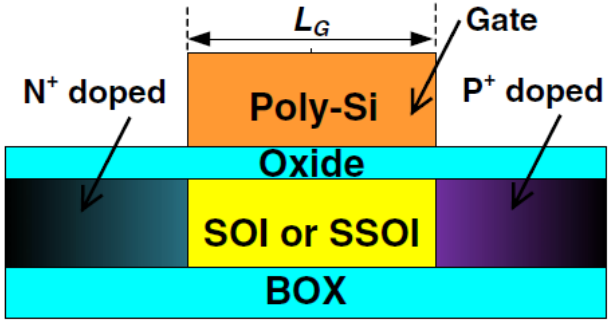
❖ **Thermionic emission**

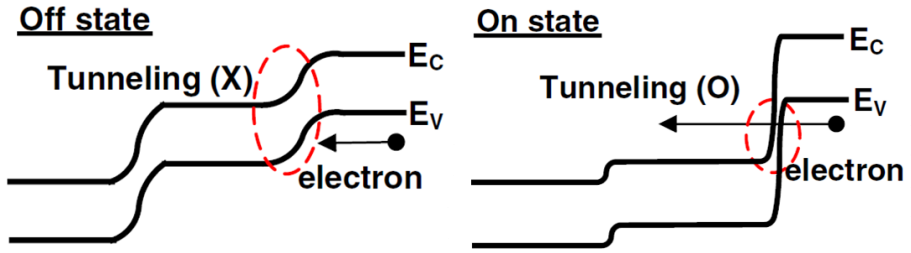
- Electrons go over the barrier



TFET

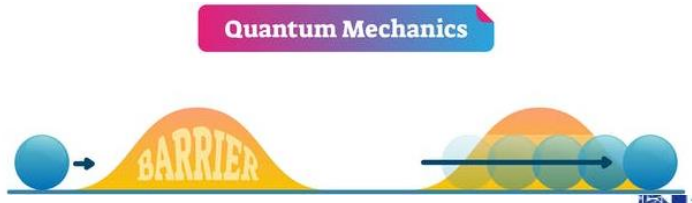
$$SS = \frac{V_{GS}^{\ 2}}{2V_{GS} + BW_g^{\frac{3}{2}}D^{-1}}$$





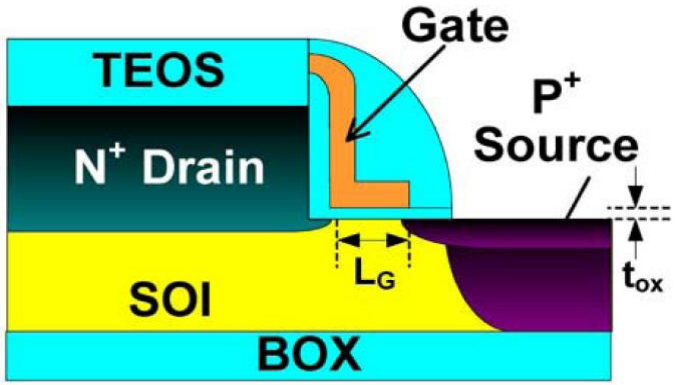
❖ **Tunneling**

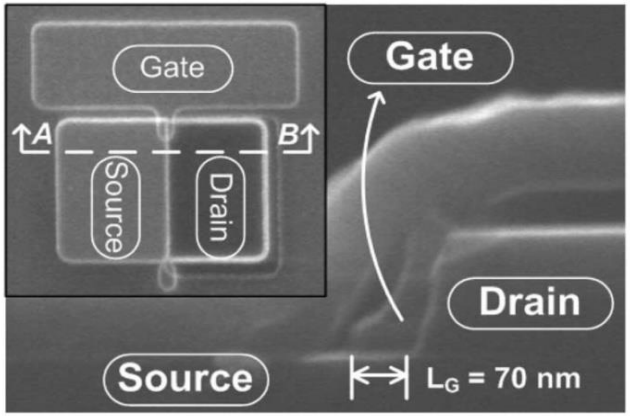
- Electrons go through the barrier

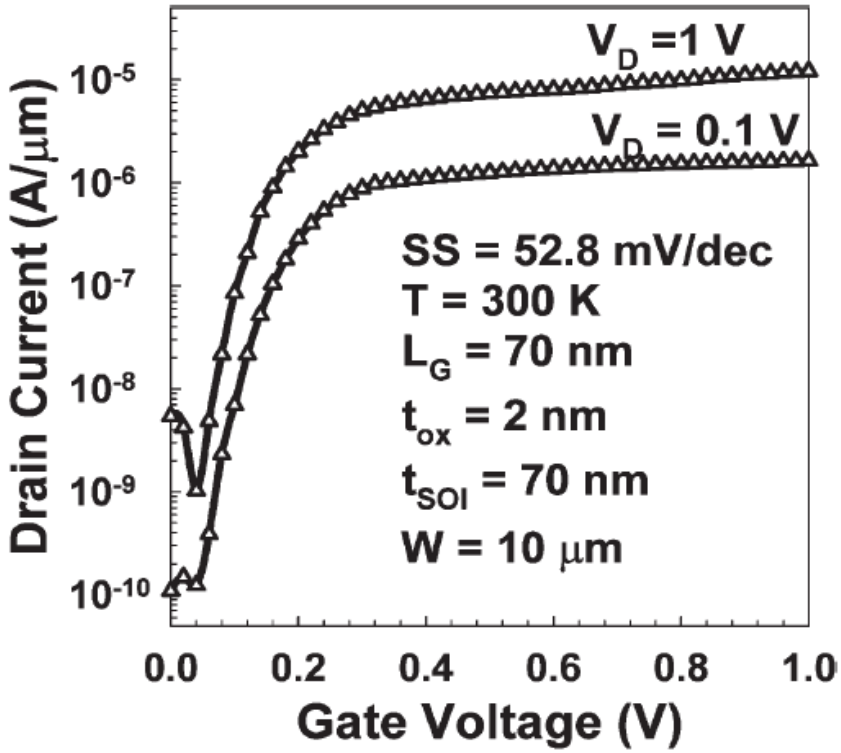


TFETs (2): Low SS & Downscaling

- First demonstration of SS < 60 mV/dec
- Downscaling (<100nm) using self-aligned process





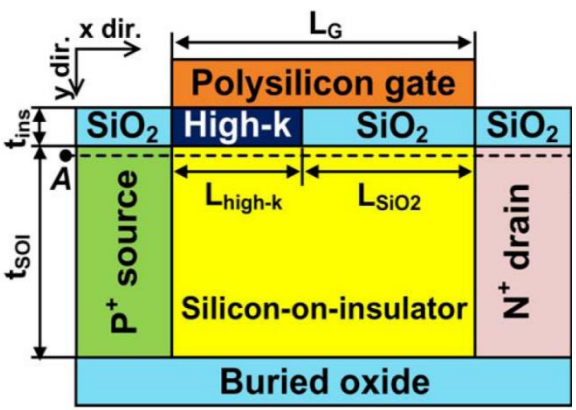


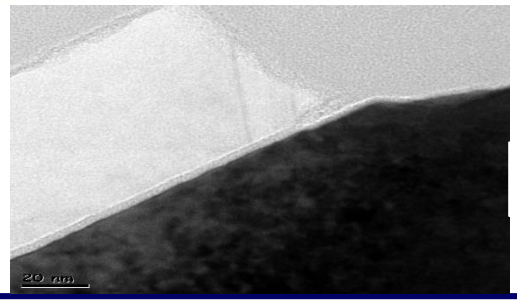
<W. Y. Choi et al., IEDM & IEEE EDL>

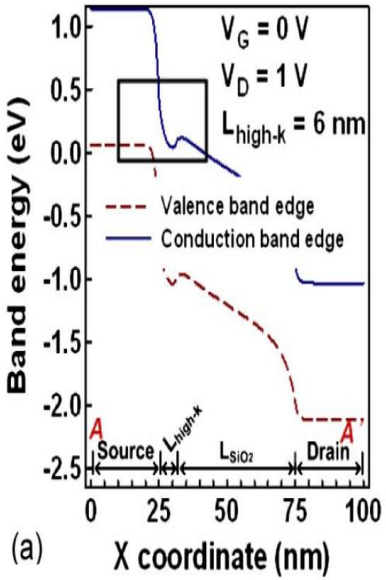
TFETs (3): On-Current Boosting

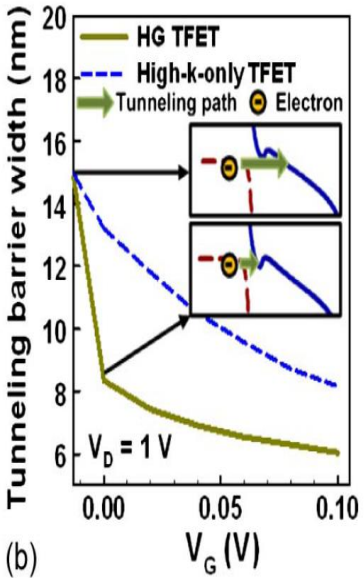
❖ Hetero-Gate-Dielectric (HG) TFETs

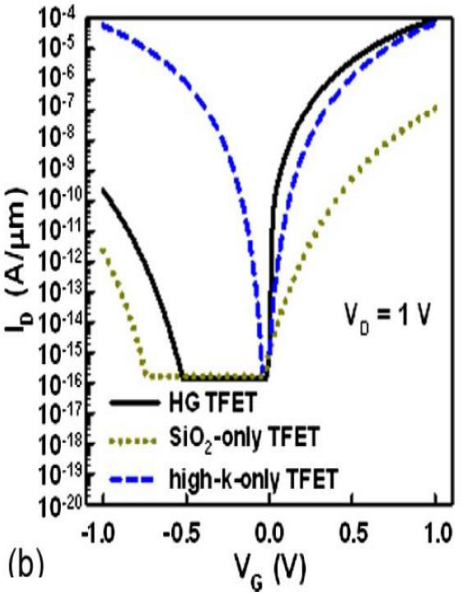
- Locally inserted high-k dielectric raises tunneling current
- Tunneling barrier abruptly narrows when a local minimum of E_C is aligned with E_V









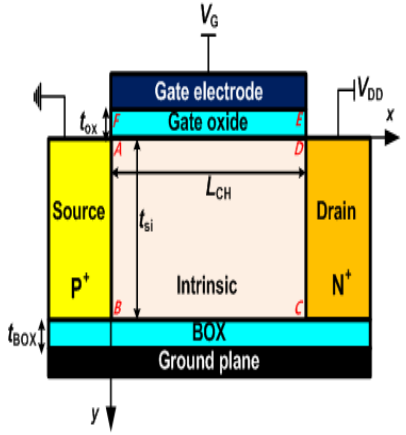


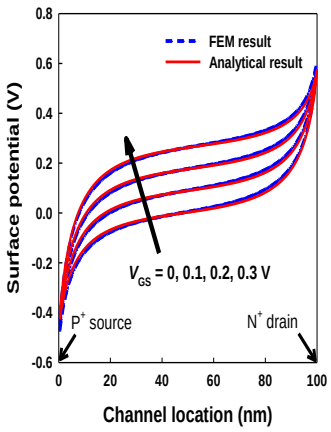
Hetero-gate-dielectric tunneling field-effect transistors
WY Choi, W Lee - IEEE transactions on electron devices, 2010
329회 인용 관련 학술자료 전체 7개의 버전

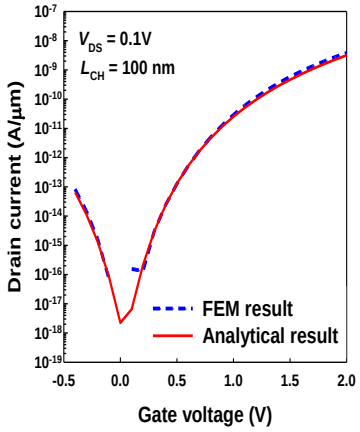
<W. Y. Choi et al., IEEE EDL & TED>

TFETs (4): Compact Modeling

First single-gate TFET compact model







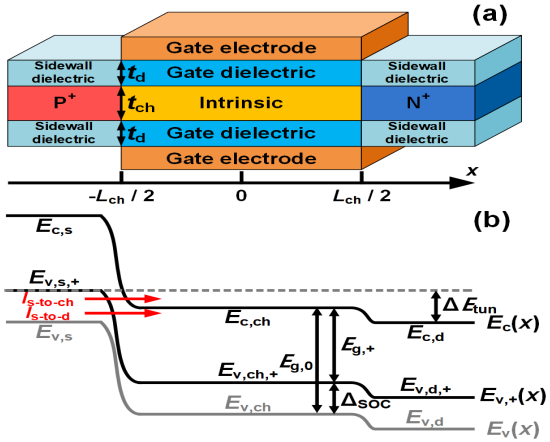
$$E_x(x,y) = -\frac{\partial\phi(x,y)}{\partial x} = \sum_{n=1}^{\infty} \frac{n\pi}{\lambda} \frac{\sin\left(\frac{n\pi(y+t_{ox}')}{\lambda}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\lambda}\right)} \left[b_n^* \cosh\left(\frac{n\pi(L_{CH}-x)}{\lambda}\right) - c_n^* \cosh\left(\frac{n\pi x}{\lambda}\right) \right]$$

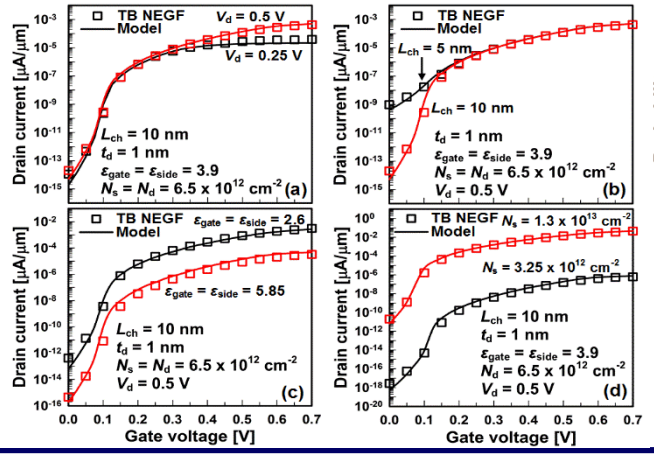
$$E_y(x,y) = -\frac{\partial\phi(x,y)}{\partial y} = \frac{\phi_s}{t_{si}} - \sum_{n=1}^{\infty} \frac{n\pi}{\lambda} \frac{\cos\left(\frac{n\pi(y+t_{ox}')}{\lambda}\right)}{\sinh\left(\frac{n\pi L_{CH}}{\lambda}\right)} \left[b_n^* \sinh\left(\frac{n\pi(L_{CH}-x)}{\lambda}\right) + c_n^* \sinh\left(\frac{n\pi x}{\lambda}\right) \right]$$

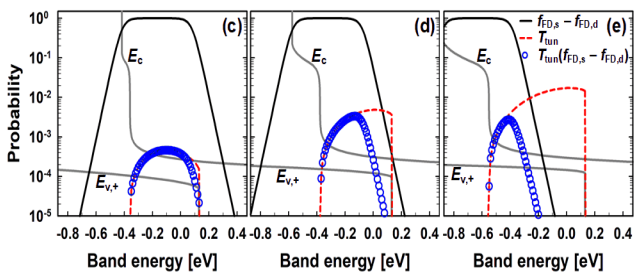
Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs)
MJ Lee, WY Choi - Solid-State Electronics, 2011
93회 인용 관련 학술자료 전체 7개의 버전

<*M. J. Lee et al., SSE*>

First 2D monolayer TFET compact model





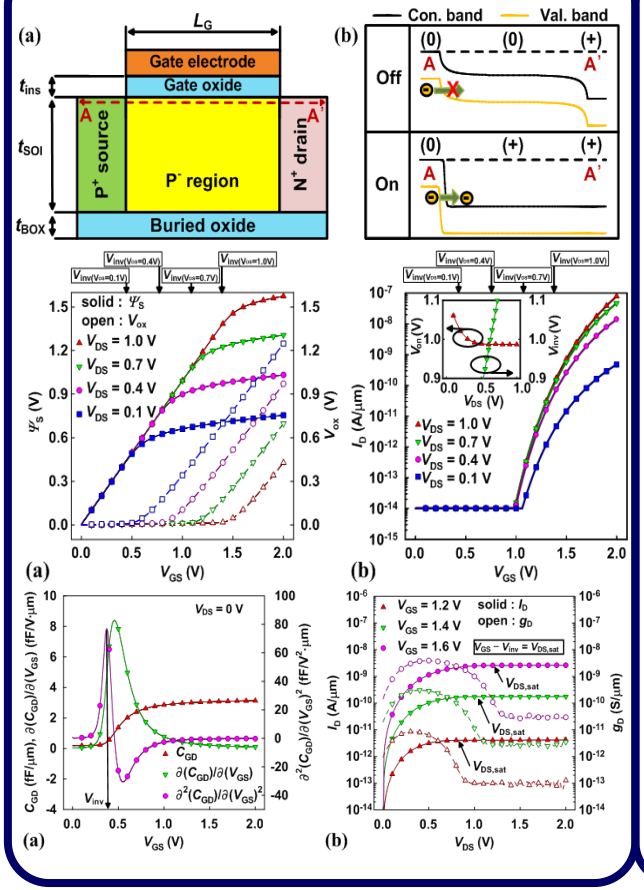


$$I_d = \frac{qg_{ts}}{4\pi^2\hbar} \int_{-\sqrt{2m_{v,+}\Delta E_{tun}}/\hbar\eta}^{\sqrt{2m_{v,+}\Delta E_{tun}}/\hbar\eta} dk_y \int_0^{\Delta E_{tun}-\eta^2 E_y} dE_x T_{tun} \left(f_{FD,s} - f_{FD,d} \right),$$

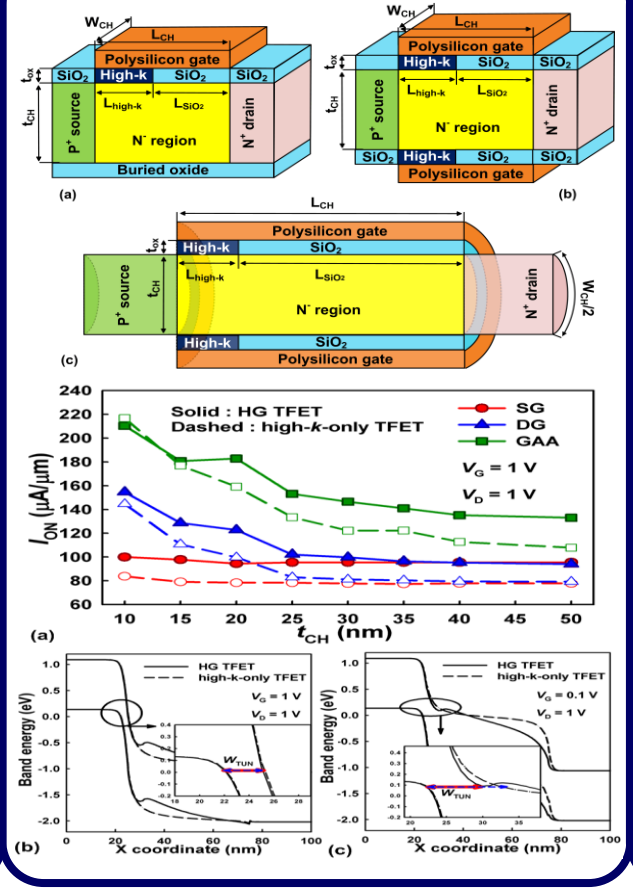
<*I. Huh et al., IEEE TED*>

TFETs (5): Physics, Structure & NVM

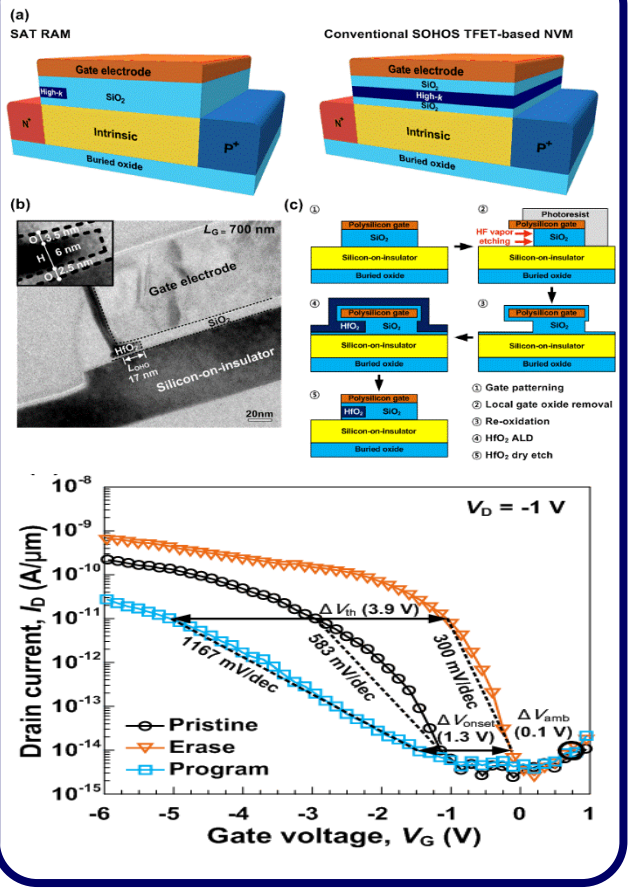
Inversion layer



Device structure



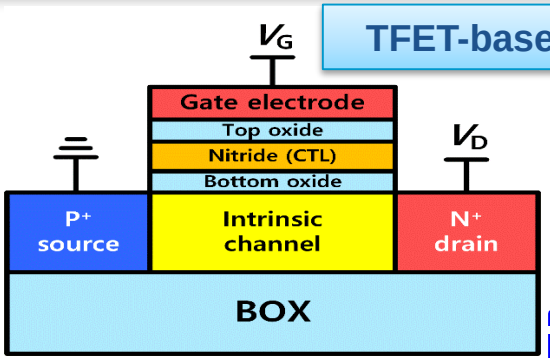
NVM



<*W. Lee et al., IEEE EDL*> <*M. J. Lee et al., IEEE EDL*> <*I. Huh et al., APL*>

TFETs (6): Synaptic Transistors

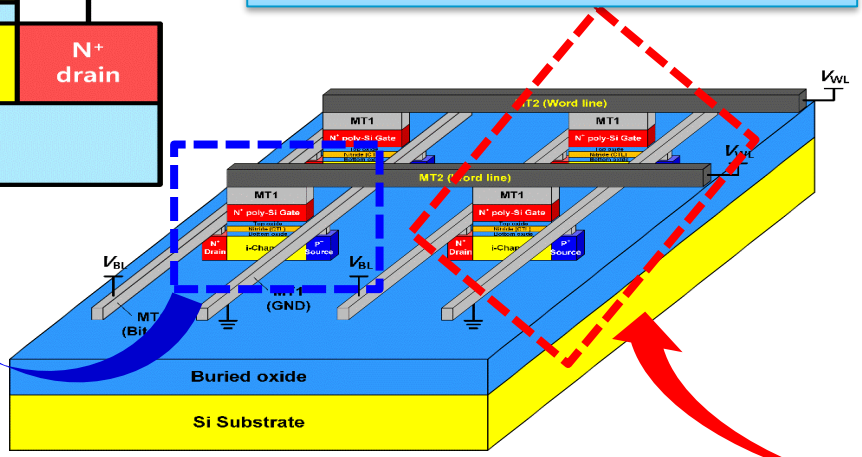
TFET-based synaptic transistor



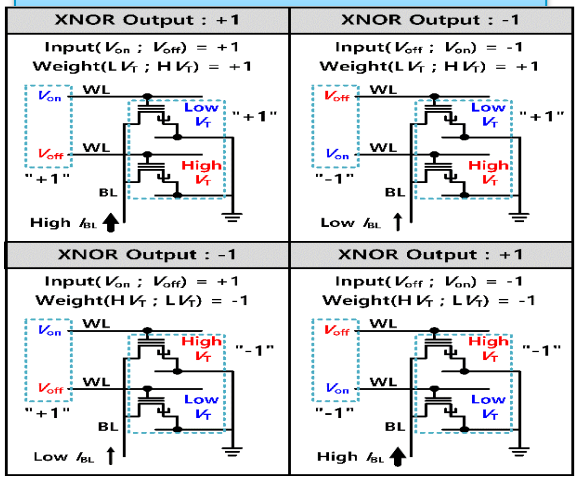
High program efficiency
Low on-current

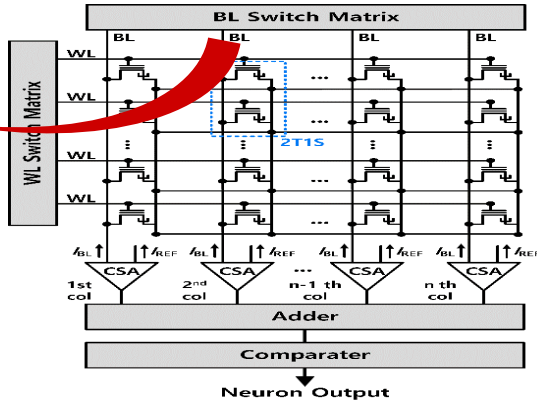
Good for synaptic transistors

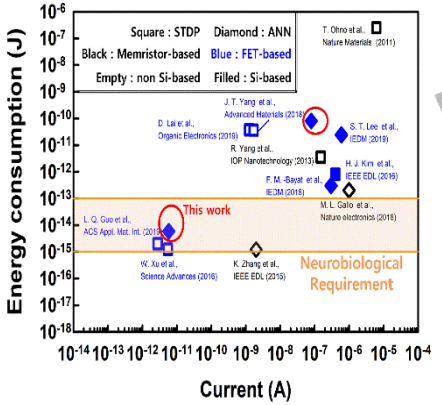
2T unit cell for XNOR operation

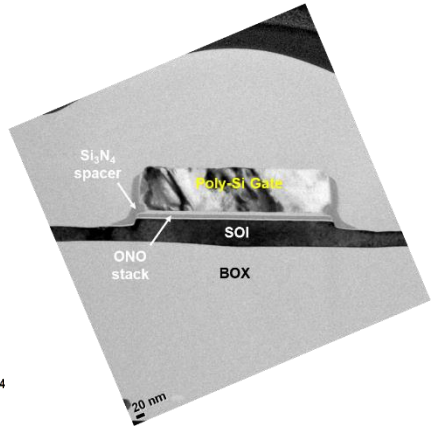


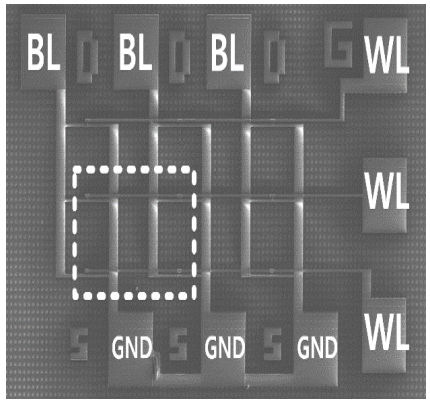
TFET-based synaptic array







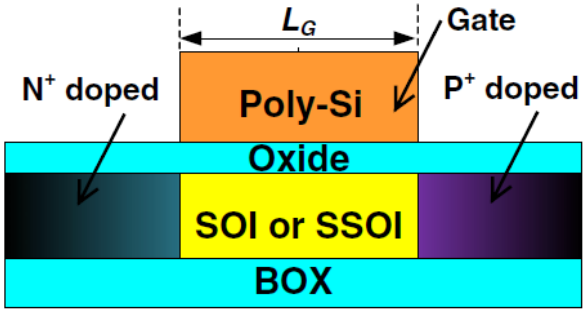




<J. W. Lee et al., IEEE EDL>

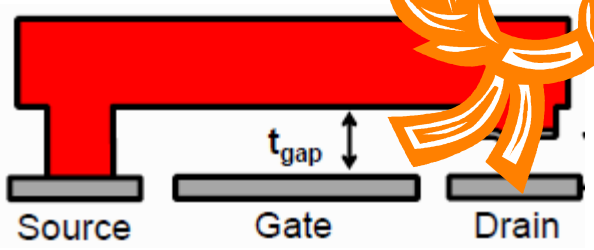
Abrupt Switching Devices

Tunnel FET



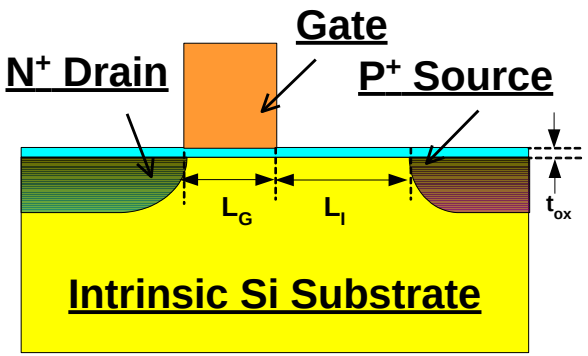
<IEDM, IEEE EDL ...>

NEM device



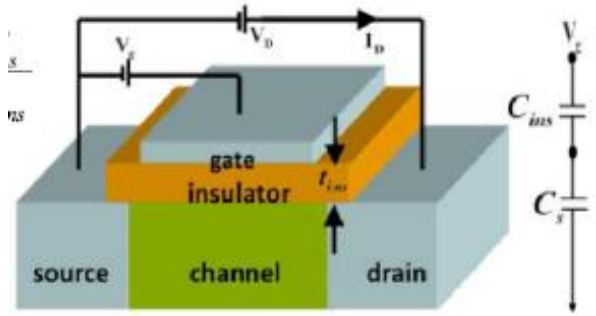
<IEDM, IEEE EDL ...>

<IEDM, IEEE EDL ...>



I-MOS

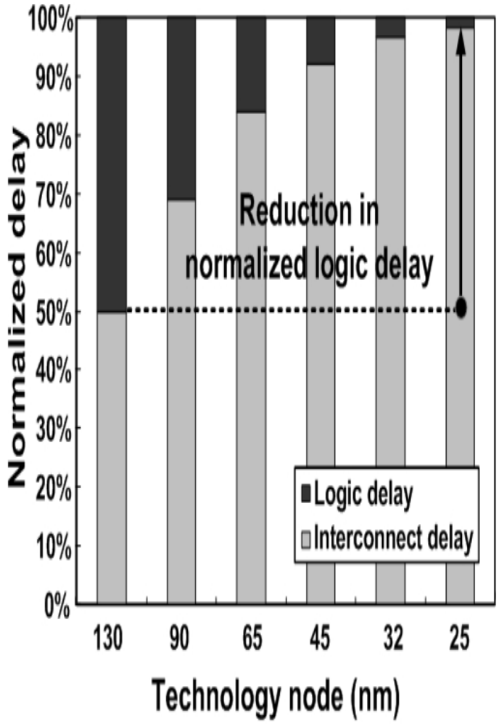
<Nano Letters ...>



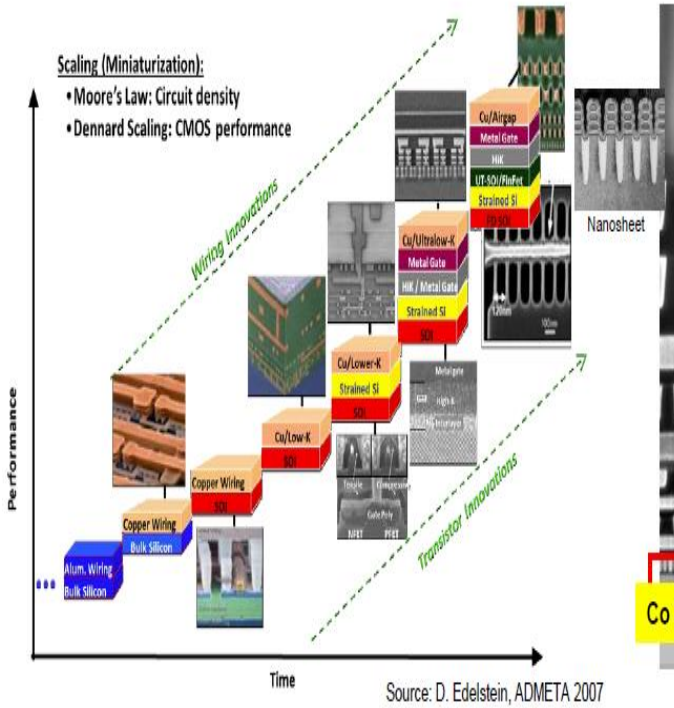
Negative cap. FET

CMOS Backend Process

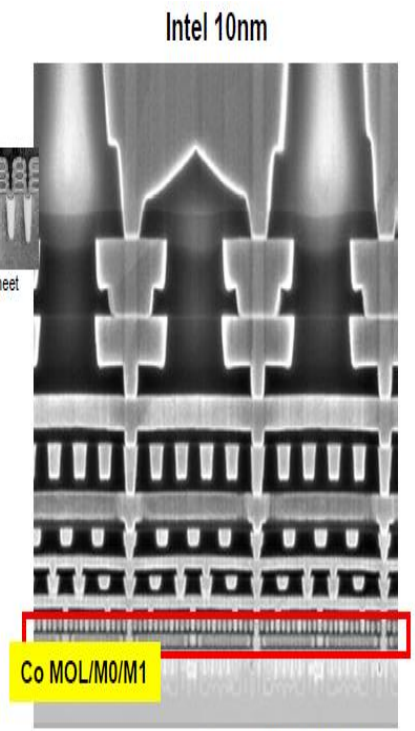
- Performance & power consumption become more dependent on CMOS BEOL than FEOL
- Increasing number of CMOS metal layers
- Introduction of air gap spacers



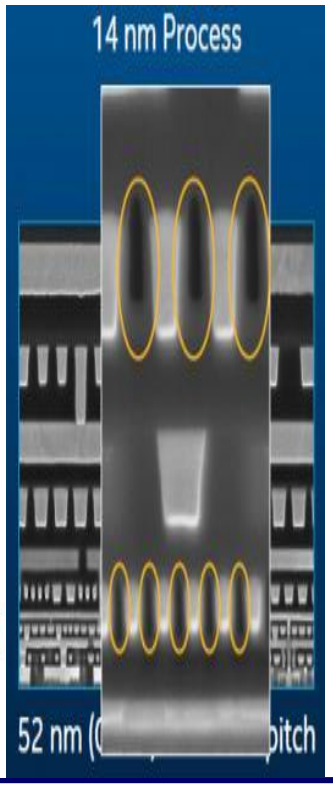
<J. Kil, et al., IEEE Trans. VLSI, 2008>



Source: D. Edelstein, ADMETA 2007



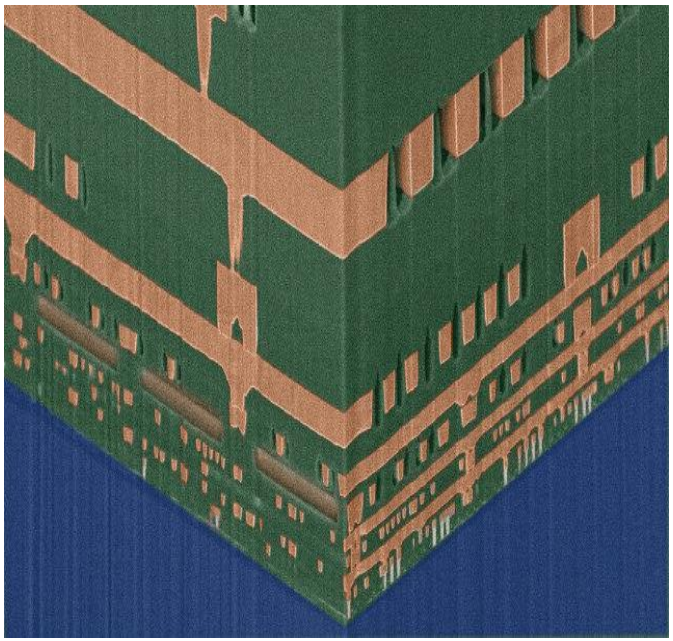
Source: C. Auth, IEDM 2017



Smart Interconnection

Conventional Interconnection

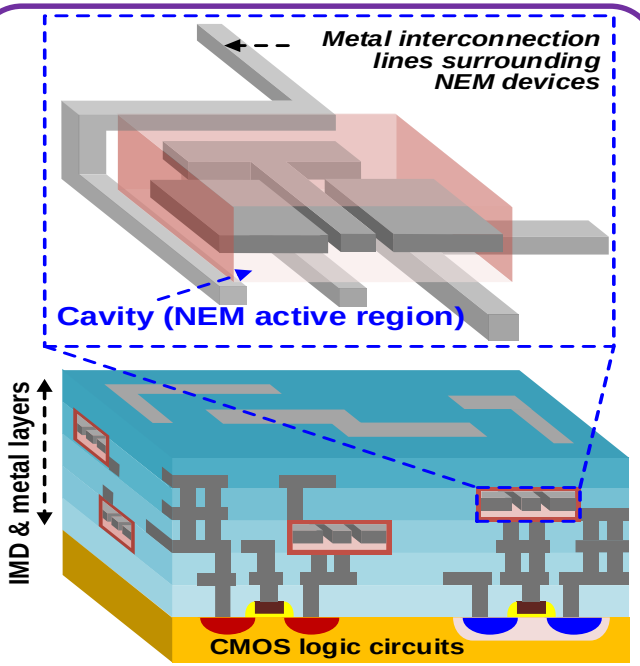
Smart Interconnection



Metal lines for passive interconnection

M3D CMOS-NEM integra-tion

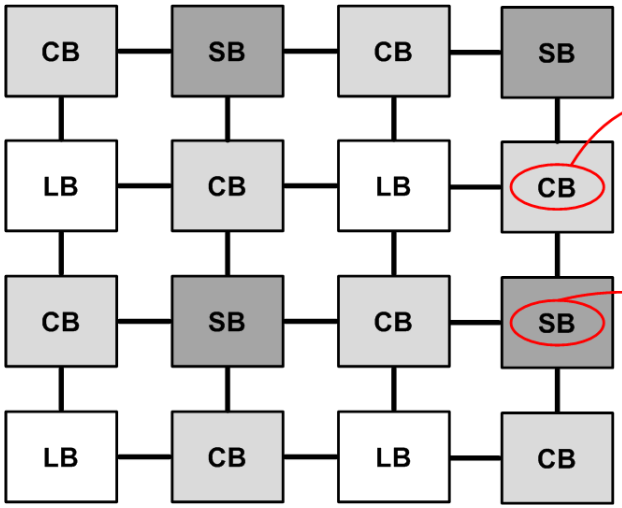
NEM = nanoelectro-mechanical

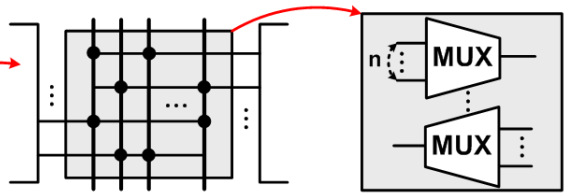


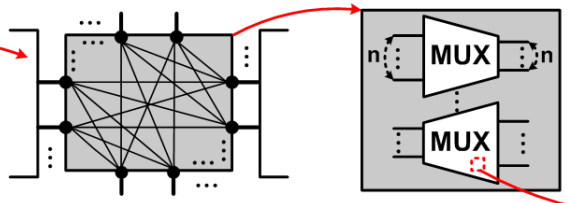
Metal lines for active devices (logic / memory / routing / sensor)

M3D CMOS-NEM: Reconfigurable Logic (1)

❖ Conventional FPGA: CMOS routing switches

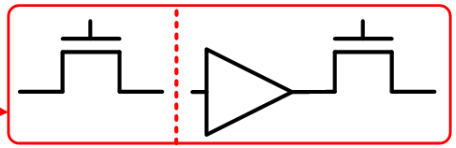


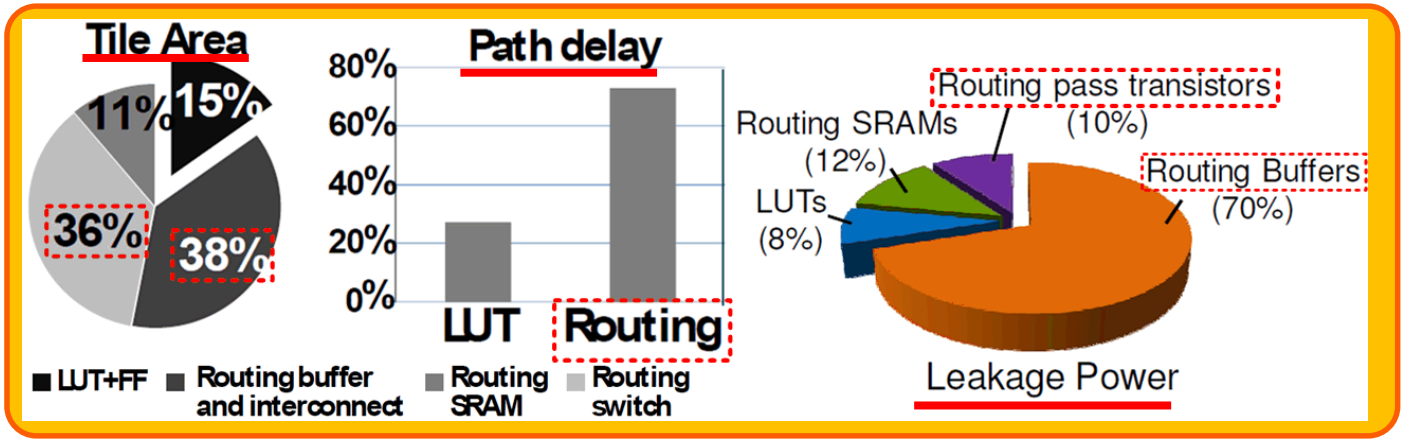




Flexibility
Development time ↓

Problem : CMOS switches

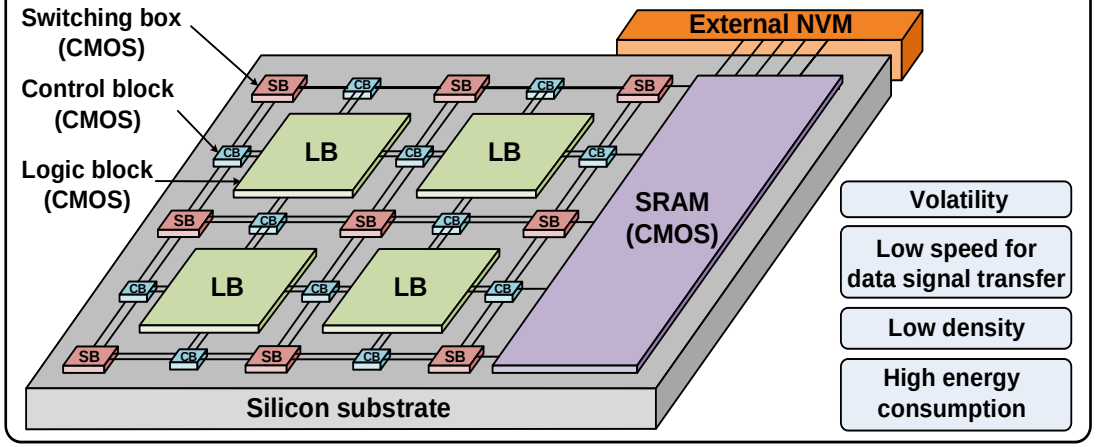




<C. Chen, et al., DATE, 2012>
<C. Chen, et al., ACM/SIGMA FPGA, 2012>

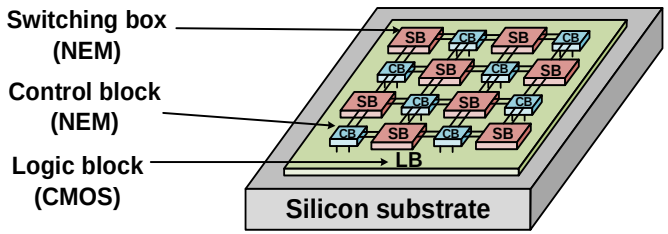
M3D CMOS-NEM: Reconfigurable Logic (2)

Conventional CMOS-based reconfigurable logic

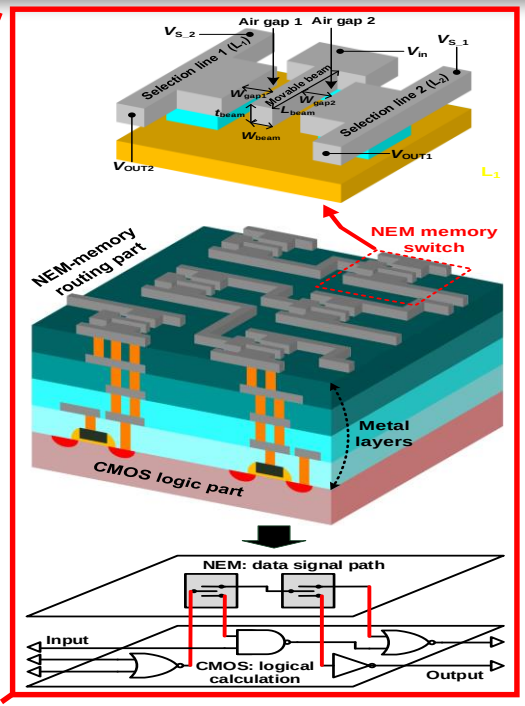


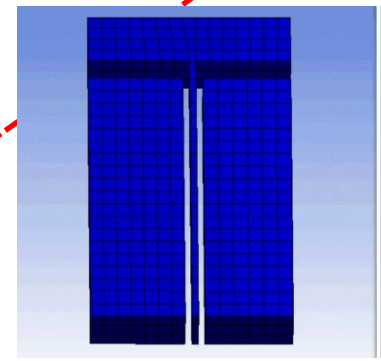
- Volatility
- Low speed for data signal transfer
- Low density
- High energy consumption

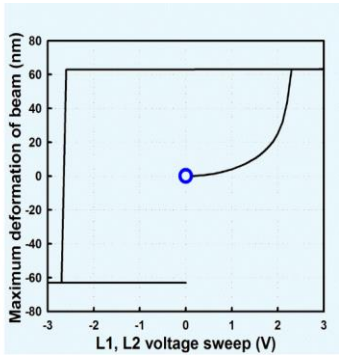
CMOS-NEM hybrid reconfigurable logic



- Non-volatility
- High speed for data signal transfer
- High density
- Low energy consumption



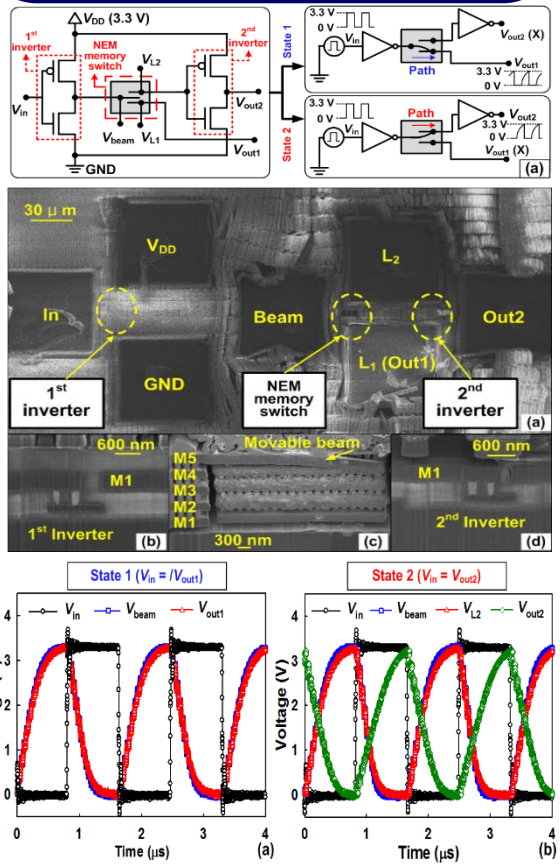




FPGAs as fast, dense, and power-efficient as ASICs

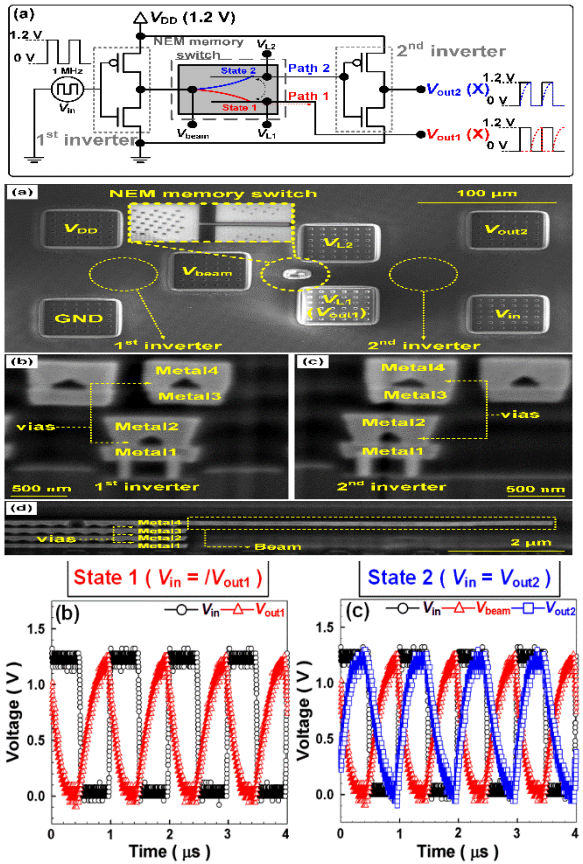
M3D CMOS-NEM: Reconfigurable Logic (3)

180nm Al process (3.3 V)



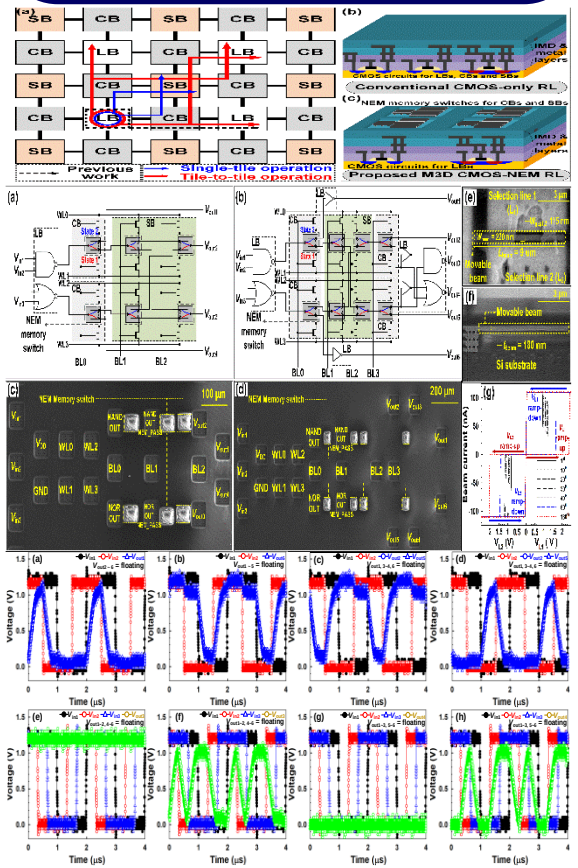
<*W.Y. Choi et al., IEEE EDL*>

65nm Cu process (1.2 V)



<*H.S. Kwon et al., IEEE EDL*>

65nm Cu process (1.2 V, Island style)



<*H.S. Kwon et al., IEEE EDL*>

Agenda

Collaboration experience with the US researchers as a post-doctor and a professor

Extremely-Low-Power Transistors

Smart Interconnection Technologies Using CMOS Backend Process

Synaptic Transistors, Neuron Circuits, and Associative Memory for Brain-Inspired Computing


Thank You !
wooyoung@snu.ac.kr